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Suppression of Short Channel Effects (SCEs) by Dual Material Gate Vertical Surrounding Gate (DMGVSG) MOSFET: 3-D TCAD Simulation

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Abstract

In this Paper, Dual Material Gate Vertical Surrounding Gate (DMGVSG) MOSFET is proposed and demonstrated using numerical simulation. In this device the features of dual material gate are adopted to get improved performance of the device. The device performance is investigated in terms of threshold voltage (Vth) roll-off, subthreshold swing (SS), drain induced barrier lowering (DIBL) and leakage current. The significance of the dual material gate is demonstrated by comparing its performance with the single material gate MOSFET. The simulation results reveal that the proposed device has suppressed short channel effects (SCEs) and improved on-current (I_{ON}). Further device exhibits improved I_{ON}/I_{OFF} ratio and low leakage current. Hence this device is an ultimate structure for future VLSI and low power applications in the nanoscale regime.

Keywords: Drain induced barrier lowering (DIBL), Dual meterial gate Vertical surrounding gate (DMGVSG), Short channel effects (SCE), Single material gate(SMG), and Subthreshold-swing (SS).

Nomenclature

N_A	Acceptor concentration (cm^{-3})
N_D	Donor concentration (cm^{-3})
V_{th}	Threshold voltage (V)
L	Channel length (nm)
d_{si}	Si pillar diameter (nm)
φ	Work function (ev)

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1. Introduction

The scaling of the conventional bulk MOSFET in the deep submicron range becomes biggest challenge in recent years. Scaling of MOSFET in nanoscale regime (<100nm) leads to undesirable effects like short channel effects and hot carrier effects, which will deteriorate the performance of the traditional MOSFET devices. The most prominent devices for nanoscale applications are multigate structures such as DGFET [1-3], FinFET [4], vertical surround gate/cylindrical gate [5-6] and gate all around structures [7-8]. These structures provide immunity against the short channel effects.

With the reduction in the channel length, the close proximity between source and drain reduces the gate control over the potential distribution and current flowing in the channel. The increased charge sharing between source and drain in nanoscale device limits further down scaling of technology parameter. The predominant short channel effects (SCEs) are V_{TH} roll-off, DIBL, Subthreshold slope, channel punch-through [9].These SCEs increases leakage current and also leads to mobility degradation.

The vertical surrounding gate (VSG) MOSFET is the promising candidate for the future VLSI applications due to its immunity against SCEs. In VSG MOSFETs silicon (Si) pillar is placed vertically on the bulk and which is used as a channel. Here source, drain and gate are stands vertically on the side walls of the pillar. VSG MOSFETs are preferred over planar MOSFETs because I) channel length is independent of the occupied area II) offers higher channel width hence higher drive current III) high speed IV) improved short channel effects. Vertical MOSFETs have great significance in the architectures like memories such as SRAM, DRAM, and EPROM. VSG structures are well suited for low power and low voltage applications.

However in vertical surround gate MOSFETs by introducing dual material gate [10-11] we can further suppress SCEs. Here two metal gates with different work functions have been used to ameliorate the performance of the device. The metal gate which is placed close to the source should have higher work function and is known as control gate. Another metal gate which is placed close to the drain is known as screen gate and should have a lower work function compare to control gate. This ensures step potential at the interface of the two metal gates, which reduces the peak electric field at the drain end, hence reduced DIBL. Dual material gate also enhances the field in the channel there by increasing the carrier mobility and hence driving capability [12].

By utilizing the benefits of both cylindrical surround gate and gate material engineering i.e. dual material gate structure a new device is proposed and simulated. And the results show superior performance of the proposed structure over conventional vertical surround gate structure.

2. Device structure and parameters

Device simulation is performed extensively by using Sentaurus TCAD, a 3-D device simulator. In this paper Single material gate VSG FET and dual material gate VSG FET are simulated and their characteristics are compared. A 3-D structures of the devices are formed using Sentaurus Structure Editor. The Devices are simulated with oxide thickness of 2nm and the channel length is varied from 20nm to 100nm.The channel is uniformly doped with the p type doping concentration of $1\times10^{16}cm^{-3}$ and n^{+} source and drain are heavily doped($1\times10^{19}cm^{-3}$). The DMG structure has two metal gates with work functions 4.9 and 4.2 ev and the corresponding materials are Co and Al. Silicon Pillar diameter is 20nm and gate materials are chosen such that the work function difference should produce a step potential at the interface of the two materials.

Table 1 Parameter values used in simulation for both the devices

Parameter	Value
Channel Length	20-100nm
Si pillar diameter	20nm
Gate work function (φ_{m1})	4.9ev
Gate work function (φ_{m2})	4.2ev
Gate oxide thickness (t_{ox})	2nm
Source/drain doping(N_D)	$1\times10^{-19}cm^{-3}$
Body doping (N_A)	$1\times10^{-16}cm^{-3}$

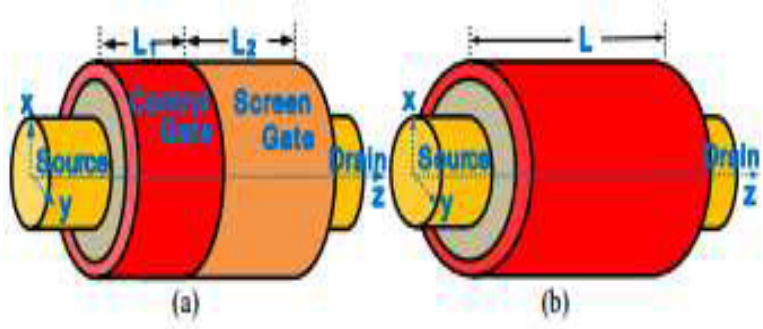

Fig 1. (a) Cylindrical channel of dual material gate VSG MOSFET. (b)Cylindrical channel of single material gate VSG MOSFET

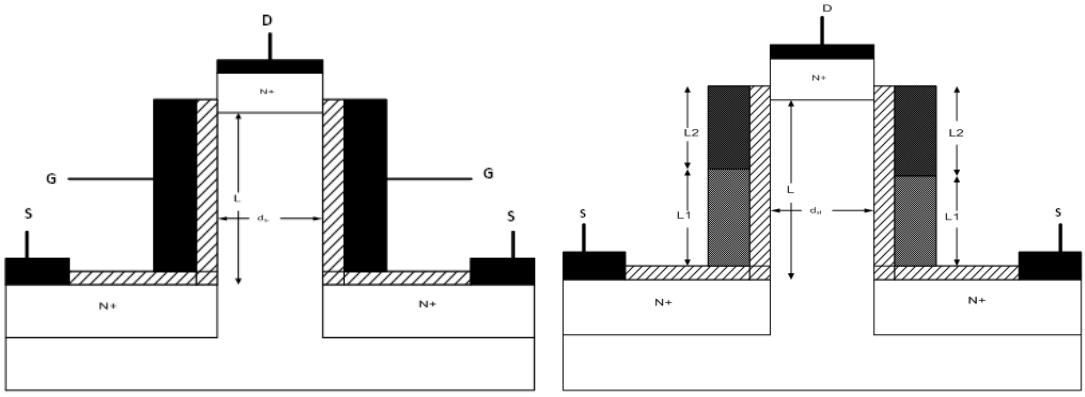

Fig. 2. Cross sectional view of simulated n-channel devices (a) SMG VSG MOSFET and (b) DMG VSG MOSFET

3. Simulation methodology

The simulations are performed using sentaurus tcad by including appropriate models such as Shockley-Read-Hall model (srh) and Auger recombination model (auger). Lattice temperature model is also activated in the simulation which is used to solve poisson's equation and heat equation. The various parameters such as threshold voltage, DIBL, off-state leakage current and on state saturation current are obtained in the simulation. Threshold voltage for different drain voltages are calculated using constant drain current method ($W/L\times10^{-7}A/um$)[13], here W is the pillar diameter and L is the channel length. The off-state current can be calculated when $V_{gs}=0$ and $V_{ds}=1V$ and it is compared in both the devices by varying the channel length.

4. Results and discussions

4.1 Subthreshold characteristics

Figure 3 shows subthreshold characteristics of the two devices for the channel length of 20nm and $V_{ds}=0.1V$. From the figure it is evident that the DMG structure has steeper subthreshold slope and lower leakage current. And it is also observed that the threshold voltage of the proposed device is higher than that of the SMG MOSFET. Due to the metal work function difference between two gates step potential is obtained at the interface. Further the peak electric field at the drain end is reduced. The mobility of charge carriers enhanced, hence the drive current.

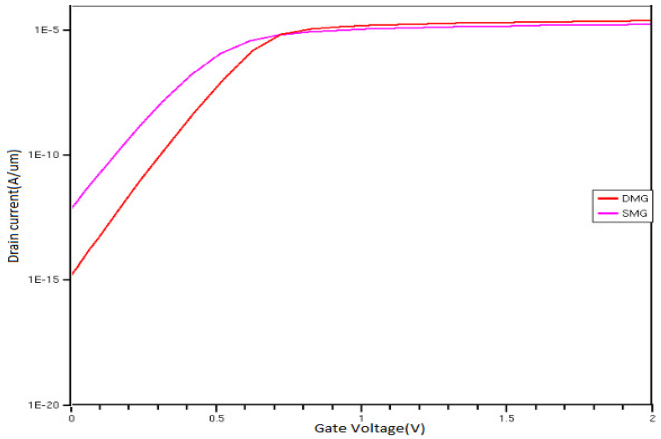

Fig. 3. Subthreshold characteristics of SMG and DMG VSG MOSFETS

4.2 Threshold voltage

Figure 4 shows the comparison of threshold voltage variation of both the devices for different channel length. There is a sharp change in V_{th} as channel length is scaled down to deep submicron range. This phenomenon cannot be observed in the proposed device due to screening effect i.e source end is screened from the variations in the drain bias voltages. The surface potential along the channel is constant with respect to change in channel length hence threshold voltage roll-off can be minimized.

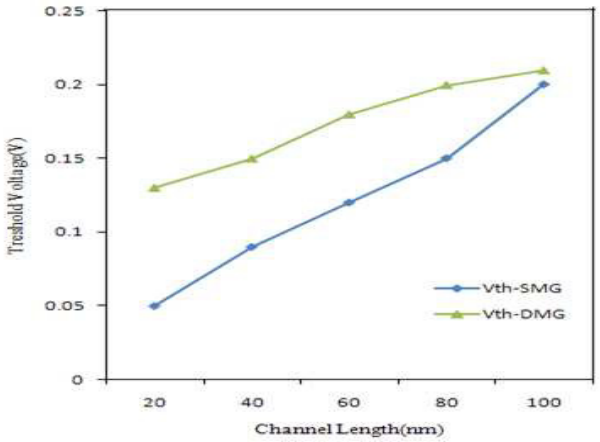

Fig. 4. Variation of threshold voltage with channel length in SMG VSG MOSFET and DMG VSG MOSFET

4.3 Drain output characteristics

Figure below compares output characteristics of devices for the channel length of 20nm. Drain voltage is swept to 2V and obtained characteristics for different gate bias voltages. In the DMG structure the drain current is enhanced over SMG structure. This is due to the fact that the gate material engineering increases surface potential in the channel at the contact of two metals, which makes the field to reallocate at the drain end. Due this the drain bias voltage has no significant effect on the inversion layer and hence no channel length modulation effect is observed in the proposed device structure. In the figure below, at higher gate bias only linear region is observed. To obtain saturation region V_{ds} should be greater than $V_{ds}(sat)$.

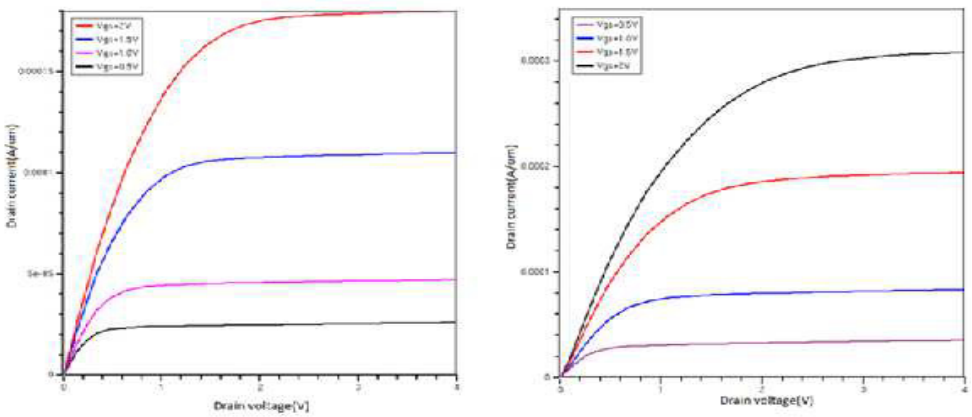

Fig. 5. Drain output characteristics of (a) SMG VSG MOSFET (b) DMG VSG MOSFET

4.4 Leakage current

Leakage current analysis performed for various channel lengths and it manifests that the proposed device has low leakage for short channel lengths. When the channel length is considered to be 20nm, leakage current of SMG structure is 9×10^{-13}A/um where as for DMG structure 4×10^{-13}A/um i.e approximately half of the SMG structure. When the channel length is considered to be 100nm both devices exhibit almost equal leakage current.

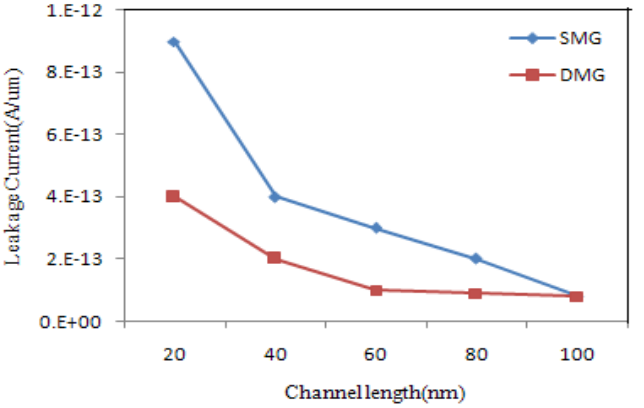

Fig. 6. Leakage current comparison of SMG and DMG VSG MOSFET for different channel lengths.

4.5 Drain induced barrier lowering(DIBL)

As the channel length shrinks, due to the close proximity between source and drain, at higher drain bias voltages the field from the drain effects the channel operation. In other words drain starts competing with gate and gate lost its control over the channel. DIBL is a measure of change in V_{th} for decade change in drain bias voltage. DIBL is calculated as [14]

$$DIBL = \frac{V_{th|V_{DS}=0.1V} - V_{th|V_{DS}=1.0V}}{V_{DS}(=1.0V) - V_{DS}(=0.1V)}$$

From the figure it can be observed that proposed architecture holds less DIBL effect due to the the reduced peak electric field at the drain end. DIBL is calculated and compared by varying the channel length.

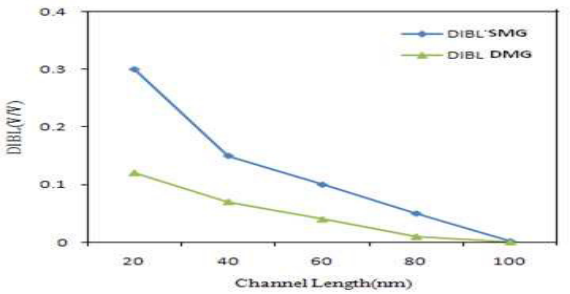

Fig. 7. DIBL variation of SMG and DMG VSG MOSFET for varying channel lengths

4.6 Subthreshold-slope

Subthreshold-slope is an important parameter in estimating performance of nanoscale devices. It can be interpreted as variation of gate voltage (V_{gs}) per decade change in subthreshold current (I_{ds}), and the minimum value is desirable. The SS variation along with the channel length is illustrated in Fig.7, and it shows that DMG exhibit improved performance over SMG structure.

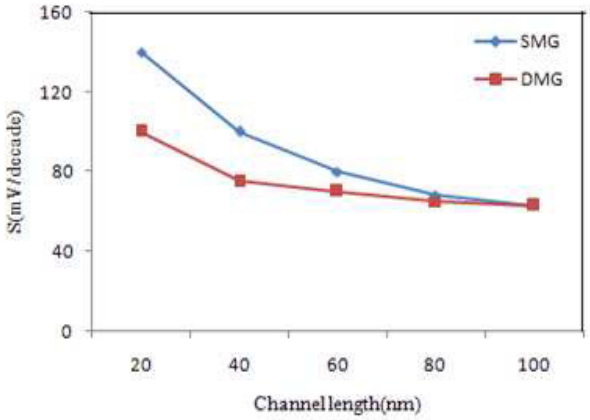

Fig. 8. Subthreshold slope variation of SMG and DMG VSG MOSFET for varying channel lengths

Conclusion

A 3-D numerical simulation of the dual material gate vertical surround gate (DMGVSG) MOSFET has been performed and compared with the single material gate vertical surround gate MOSFET. The incorporation of dual material gate resulted in significant reduction of short channel effects and improved I_{ON}/I_{OFF} ratio obtained. In the proposed device we have observed less threshold voltage variation with channel length i.e. less V_{TH}-roll off and leakage current. And improved DIBL, subthreshold slope even channel length is scaled down to 20nm. The comparisons of simulated results reveal that the proposed device is well suited for low power vlsi application in nanoscale regime.

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